

# **Geometrical Parameters Optimization and Microwave Characterization of Graphene-Based Transmission Lines**

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**تحسين المعلمات الهندسية وخصائص الموجات الميكروويف لخطوط النقل القائمة على الجرافين** 

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Received: September 05, 2024 | Accepted: October 28, 2024 | Published: December 22, 2024 **Abstract:** 

This study addresses the need to reduce circuit size in integrated circuits, the growing use of monolithic microwave integrated circuits (MMICs) in wireless applications, and the demand for high performance. It investigates the relationship between graphene microstructures and high-frequency behavior by modeling their microwave response through electromagnetic simulations and validating results with on-wafer measurements. The impact of skin depth on microwave performance is specifically examined. Graphene coplanar transmission lines (CPWTLs) were fabricated on silicon wafers and characterized in the 2-20 GHz range. Initial analysis using a CST electromagnetic simulator optimized geometric parameters and predicted RF performance. The optimal structure was fabricated with standard semiconductor techniques and evaluated with a Cascade Microtech probe station connected to a vector network analyzer (VNA). Measurements up to 20 GHz show that graphene maintains consistent properties across the bandwidth with negligible skin effect, outperforming other studies.

**Keywords:** MMIC, CPWTL, VNA, CST, Skin effect.

**الملخص** 

تتناول هذه الدراسة الطلب المتزايد لتقليص حجم الدوائر في تكنولوجيا الدوائر المتكاملة، وزيادة تبني الدارات الميكروويف المتكاملة المونوليثية *(MMICs (*في التطبيقات الالسلكية، والحاجة إلى األداء العالي. تستكشف الدراسة العالقة بين الهياكل الدقيقة للجرافين وسلوك الترددات العالية من خالل نمذجة استجابة الترددات الميكروويفية باستخدام المحاكاة الكهرومغناطيسية والتحقق من النتائج من خالل القياسات على الرقاقة. على وجه الخصوص، تفحص الدراسة تأثير عمق الجلد على أداء الميكروويف. تم تصنيع خطوط النقل المتوازية للجرافين *(CPWTLs (*على رقائق السيليكون وتم تعريفها ضمن نطاق التردد من 2 إلى 20 جيجاهرتز. تم إجراء تحليل أولي للعديد من التكوينات باستخدام محاكي الكهرومغناطيسية *CST* للتنبؤ باألداء الترددي وتحسين المعلمات الهندسية. تم تصنيع الهيكل ا ألمثل باستخدام تقنيات معالجة أشباه الموصالت القياسية، وتم تقييم خصائصه باستخدام محطة قياس من *Microtech Cascade* متصلة

بمحلل شبكة متجهية *(VNA(.* أظهرت قياسات معامالت االنتثار حتى 20 جيجاهرتز أن الجرافين يحتفظ بخصائص ثابتة عبر النطاق التردد*ي مع* تأثير ضئيل للجلد، متفوقًا على النتائج الواردة في دراسات أخرى.

**الكلمات المفتاحية: دوائر** متكاملة أحادية الموجات الدقيقة، محلل الشبكة المتجهة، تأثير الجلد*.*

## **Introduction**

Graphene, though a relatively recent discovery, has shown considerable potential for a variety of applications in next-generation electronic devices [1]. Since its isolation in 2004 through mechanical exfoliation of highly ordered pyrolytic graphite (HOPG), carbon-based materials have drawn renewed attention in nanoelectronics [2]. Graphene's two-dimensional planar structure is compatible with the same processing technologies as silicon, making it suitable for integration. In monolithic microwave integrated circuits (MMICs), passive components, particularly distributed elements like transmission lines, require significant wafer space during fabrication [3]. With the rapid development of wireless technology, MMIC circuit sizes are shrinking, reducing the space available for passive components and driving their dimensions down to the nanometer scale. Currently, copper, gold, and aluminum are the primary materials used for MMIC transmission lines [3, 4].However, as these materials approach their physical limits, resistance increases while performance decreases, posing challenges for MMICs and limiting their use in modern communication systems [5]. Graphene has been identified as a potential alternative due to its favorable electrical properties, including high carrier mobility, high current density, excellent thermal conductivity, and micron-scale mean free paths [6–9]. Additionally, graphene exhibits minimal skin effect and maintains nearly constant impedance across a wide frequency range [10, 11]. Although various studies have investigated graphene's use in microwave applications [12–16], most have focused on its role as a semiconductor to replace silicon in the carrier channel between the source and drain of transistors [17–19]. Research into the use of graphene as a material for MMIC transmission lines has been relatively limited [20, 21]. This paper proposes the use of graphene as an alternative material for MMIC transmission lines, addressing the challenges posed by conventional materials and leveraging graphene's unique properties to enhance performance in microwave applications.

## **Methodology**

The methodology begins with identifying the need for high-performance microwave transmission lines, focusing on graphene due to its exceptional electrical properties, such as high carrier mobility and low resistivity. The geometrical parameters of the CPWTL are optimized through CST simulations to achieve a characteristic impedance of 50 Ω. The fabrication process involves substrate preparation, graphene deposition, photolithography, etching, metal contact deposition, and annealing, followed by inspection to ensure quality. Experimental validation is conducted using on-wafer measurements with a Vector Network Analyzer (VNA) across 2–20 GHz to assess performance. Finally, simulation and measurement results are analyzed to evaluate the suitability of graphene-based CPWTLs for MMIC applications.

# **Parameter Justification**

- 50 Ω Impedance: Ensures compatibility with standard RF and microwave components.
- Graphene Material: Chosen for its high carrier mobility, negligible skin effect, and suitability for high-frequency operations.
- Substrate: Silicon offers a reliable and cost-effective base for fabrication.
- Frequency Range (2–20 GHz): Selected to validate CPWTL performance across a broad spectrum.

## **Graphene test structure simulation**

Microwave circuits commonly utilize various architectures, such as co-planar waveguide (CPW), microstrip, slotline, and stripline. Among these, the CPW geometry was chosen to efficiently transfer high-frequency signals from the microwave probe to the graphene sample. This selection was primarily due to CPW's compact design, which is well-suited for MMIC integration, its low dispersion, ease of accommodating lumped elements in different configurations, and the absence of via holes required for ground plane access in the substrate [22–24].

A standard co-planar waveguide (CPW) consists of a central conducting strip flanked by two ground conductors, separated by gaps on the same substrate surface [23, 24]. Figure 1 illustrates the schematic of a CPW structure, which comprises a patterned conductor strip with dimensions t, w, and l. This structure is supported by a Si/SiO2 dielectric layer of thickness h and relative permittivity εr. The central conductor is responsible for carrying the signal, while the two adjacent conductors function as ground planes.



**Figure 1**: Schematic of a Coplanar Waveguide Structure

## **A. Effect of Line Geometry**

The geometrical parameters w and s were optimized using CST software to achieve an input impedance of 50 Ω. The structure consisted of 3 nm-thick graphene layers, a 500 nm SiO2 layer, and a 500 μmthick Si substrate. The Si substrate had a relative permittivity of 11.9 and a conductivity of 1 S/m, while the SiO2 layer exhibited a relative dielectric constant of 3.9 and an electrical conductivity of 1×10−13 S/m. The device was designed with a characteristic impedance of 50  $\Omega$ , the standard for microwave devices, to maximize signal transmission through the coplanar waveguide and minimize reflections at the input port [25, 26]. The simulation for determining the line impedance begins with a simple symmetrical design, featuring an ungrounded CPW layout. The conductor width w and a 50 μm gap between the center conductor and the ground planes are used. These dimensions are selected to align with the probe station size on the wafer connected to the vector network analyzer. Figure 2 illustrates the design.



**Figure 2**: 50 μm width and gap symmetrical CPW layout simulation.

The line impedance shown in Figure 2 was approximately  $41\Omega$ . The actual impedance value is then refined by adjusting the dimensions of the transmission line [25, 26]. Several CPW lines with varying gap sizes were simulated, while the signal and ground line widths were fixed at 30 and 50 μm, respectively. The structure is presented in Figure 3. The computed impedances for two simulation results are shown in Figures 4 and 5. The minimum line width was set to 10 μm due to the limitations of the lithography and etching techniques used in this study.



**Figure 3:** CPW Layout with Fixed Width and Varying Gaps





**Figure 5:** CPW Layout with 70 μm Fixed Gap Width. 42.9 was the calculated line impedance.

The simulated line impedance increased from 38.69  $\Omega$  to 42.89  $\Omega$  when the gap expanded from 30 µm to 70 μm, as shown in Figure 4 and 5 and Table 1.



# **B. Layout Optimization**

To align with the probe footprints, the layout was further refined to adjust the line impedance closer to 50 Ω, while considering the constraints imposed by the probe contact pad size and pitch. The simulated  $|S_{11}|$  and  $|S_{21}|$  in dB for the CPW lines are displayed in Figure 6, where the gap (s) and width (w) vary from 50 to 105 μm and 10 to 50 μm, respectively.



Figure 6: Simulated S<sub>11</sub> and S<sub>21</sub> for CPW with Varied w and s

## **Results and Discussion**

One of the key findings from Figure 6 is that the line width w influenced the S-parameters. As seen when w increased from 10 to 20  $\mu$ m, widening the line reduces  $S_{11}$  and increases  $S_{21}$ . This indicates a reduction in reflected signals at the CPW line's input ports and an increase in power transmission to the output ports.

Additionally, it is important to note that  $S_{21}$  changed significantly when w increased from 10 to 20 µm. However, when w increased from 30 to 40 µm,  $S_{21}$  only showed a slight change. Between 40 and 50 µm, S<sup>21</sup> remained nearly constant. Finally, when the spacing was adjusted while keeping the line width w constant, there was no change in the S-parameters. This indicates that the line impedance is primarily determined by w, rather than s [27]. Table 2 presents the calculated line impedance for the CPW with different line widths and ground-to-ground distances (w+2s).





With the sum of w and s taken into account, Table 2 displays an intriguing pattern in which the line impedance and the line width are related. Wider lines with smaller gaps s will produce lower impedance when  $w + s = 100 \mu m$  (fixed), which is to be expected since the line impedance will decrease as the line widens [28]. Conversely, when w + s  $\neq$  100 µm, wider lines with smaller gaps will produce higher impedance. Table 2 reveals that the line with a 20 µm width and an 80 µm gap provides the impedance closest to the 50  $\Omega$  characteristic impedance. However, as shown in Figure 6, it also exhibits a higher insertion loss. Therefore, the optimal values for a 50  $\Omega$  line are w = 30 µm and s = 75µm. The ideal size and corresponding impedance for the graphene CPW are shown in Figure 7.



**Figure 7:** The computed line impedance and the final CPW's dimensions.

The signal and ground electrodes each have a width of 30 μm, a gap of 75 μm, and a length of 250 μm. The CPW structure features three gold contact pads at each end of the electrodes, which serve as measurement footprints for the on-wafer probe. The gold pads have a thickness of 60 nm. S-parameter plot of the ideal CPW as simulated by the CST simulator in the 2 GHz–20 GHz band. Figure 8-a plots simulations  $|S_{11}|$  and  $|S_{21}|$  on a logarithmic dB scale. Figure 8-b displays the port signal results.



(b)

**Figure 8**: The optimised CPW's (a) simulated S-parameters and (b) port signals.

The curves in the port signals graph show that the incident and transmitted signals have nearly the same magnitude and phase, while the reflection is 90° out of phase and has a relatively small magnitude. Over most of the frequency range, the input reflection  $S_{11}$  is quite low (less than 20 dB), suggesting that almost all the power was transmitted to the output and only a minimal amount of the signal was reflected at the CPW input. As expected, the scattering parameter results align with the port signal observations.

## **Graphene RF Characterization**

Test structures were fabricated from graphene films in the form of coplanar transmission lines using electron beam lithography to facilitate high-frequency characterization and simulate their function as interconnects. The fabrication process details are discussed in [29, 30]. The coplanar transmission line measures 250 μm in length and 30 μm in width. S-parameters, obtained using an R&S ZVA40 vector network analyzer and Cascade Microtech probes, were used to determine the transmission and reflection properties as illustrated Figure 9.



**Figure 9:** Cascade Microtech probes.

The full transmission and reflection properties of each sample at a particular frequency are provided by the S-parameters of the CPW measured here, "S $_{11}$ " and "S $_{21}$ ." Measurements of two-port reflection were conducted between 2 and 20 GHz. Figure 10 displays the measured line values for  $|S_{11}|$  and  $|S_{21}|$ on the logarithmic dB scale.

It is evident that the  $S_{21}$  trace shows a reduced capacity for microwave transmission. The lengthy etching procedure used to manufacture the device is probably the cause of this deterioration. Since the substrate is significantly thicker than the film and electrons are dispersed by optical phonons in highfrequency IC devices, substrate losses naturally also have an impact on the  $S_{11}$  and  $S_{21}$  values. These losses account for the majority of signal losses in high-frequency IC structures. The quality of pattern mobility is influenced by the substrate. Additionally, line edge roughness and contamination dispersion have an impact on the transmitted signal.



**Figure 10:** Measured  $|S_{11}|$  and  $|S_{21}|$  Values

It is also important to note that, compared to conventional conductors, the skin effect is negligible, as the majority of losses are due to the base material. Overall, the findings align with previous research [31–33]. For example, the average transmission level at 20 GHz for the sample in this study is approximately 3 dB greater than the value given in [33] and roughly 5 dB higher than the average transmission level reported in [31]. This suggests that, given the thickness of the graphene layer utilised, the graphene-CPWTL under investigation shows improved RF performance. In order to minimise attenuation caused by conductor losses, the conductor thickness should be at least five times the penetration depth [34, 35]. The graphene film used in this study has a thickness of approximately 3 nm, which is much smaller than the skin depth at GHz frequencies, yet the results show that graphene is not significantly affected by the skin effect.

## **Conclusion**

Graphene-based CPW test structures were thoroughly investigated in this experimental study using a microwave frequency range of 2 to 20 GHz. In order to forecast RF performance and optimise geometric characteristics, the test structures were first simulated using an electromagnetic simulator. A wafer probe attached to a VNA was then used to pattern and measure the structures in order to determine the S-parameters. When compared to other studies, the results demonstrated better performance. The conclusion is that graphene is a material that works well for MMIC structures. According to the results, graphene may be used to create thinner and smaller MMIC gearbox lines without sacrificing performance when compared to traditional MMIC materials. The graphene-metal contact had the biggest impact on graphene's impedance, suggesting that more research on the graphene-metal structure is required to enhance performance. To fully investigate graphene's potential, measurements might be expanded up to 100 GHz. This would increase the material's applicability in other MMIC components such filters, amplifiers, resonators, and switching circuits, as well as for greater bandwidth applications. Since substrate loss accounts for the majority of signal losses in high-frequency integrated circuit architectures, a high-resistivity Si substrate should be used to accomplish this. Up to tens of GHz, high-resistivity Si substrates do not depend on frequency.

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